Abstracts

A direct-conversion W-CDMA front-end SiGe receiver chip

D.Y.C. Lie, J. Kennedy, D. Livezey, B. Yang, T. Robinson, N. Sornin, T. Beukema, L.E. Larson, A. Senior, C. Saint, J. Blonski, N. Swanberg, P. Pawlowski, D. Gonya, X. Yuan and H. Zamat. "A direct-conversion W-CDMA front-end SiGe receiver chip." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 31-34.

A W-CDMA direct-conversion front-end receiver chip consisting of a low-noise amplifier (LNA), a dual-gain RF variable-gain amplifier (RF-VGA), two direct-down-conversion mixers, a I/Q quadrature generator, and a base-band five-gain-stage VGA is designed and manufactured in a 0.25 /spl mu/m IBM SiGe BiCMOS production process. A very low DC offset value (<300 /spl mu/V) is measured at the output of the mixers as the LO signal is fed into the chip at twice the RF frequency. An extremely low local oscillator (LO) leakage of -105 dBm is measured at the LNA input, partly due to the excellent LO-to-RF isolation provided by the RF-VGA and the direct-conversion mixers. The measured cascaded noise figure for the chip (including the SAW filter) is 4.3 dB at the maximum gain mode, and the IIP2 and IIP3 are +37 and -16.5 dBm, respectively. The I/Q channels exhibit a small mismatch in magnitude (<0.1 dB) and in phase (1/spl deg/-1.5/spl deg/). The chip draws 24.9 mA from a 2.85V supply. The overall chip performance meets all the essential parameters of W-CDMA receiver front-end specs.

❑ Return to main document.